CHAPTER 6

CONTROL OF NEUTRAL POINT VOLTAGE

6.1 Introduction

One of the major drawbacks of the multilevel converters is the neutral point voltage problem. For a proper operation of multilevel converters, it is imperative that the dc bus voltages are divided equally between the capacitors. In case of three-level converter, each capacitor has to be maintained at half the dc-bus voltage. Proper control techniques have to be used to ensure the neutral point voltage to be maintained at zero. There are several reasons for the neutral point voltage imbalances such as the unequal capacitances of the capacitors due to manufactures tolerance value, asymmetrical layout, nonlinear loads, etc. One of the solutions for solving this neutral point voltage imbalance problem is by using bulk capacitors. This is not a feasible solution as it increases the cost of the converter. Hence the choice of modulation scheme becomes important in controlling the neutral point voltage.

6.2 Control of Neutral Point Current using Carrier-based PWM

The carrier-based PWM technique using single carrier and multiple modulation signals is explained in Chapter 4. The extension of the PWM scheme to control the neutral point current using the concept of sharing functions is presented in this section.

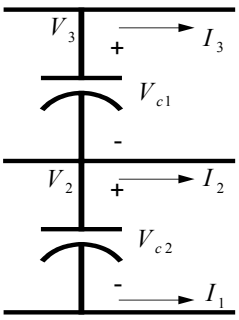


Figure 6.1: Node currents of three-level converter.

6.2.1 Three-level Inverter

The node currents for a three-level inverter are given by

$$I_3 = H_{a3} i_a + H_{b3} i_b + H_{c3} i_c \tag{6.1}$$

$$I_2 = H_{a2} i_a + H_{b2} i_b + H_{c2} i_c \tag{6.2}$$

$$I_1 = H_{a1} i_a + H_{b1} i_b + H_{c1} i_c . \tag{6.3}$$

The node current I_2 is known as the neutral current. Whenever there is an imbalance in the capacitor voltages, due to the potential difference, the current through node 2 will flow into or out of the converter depending on the polarity of the neutral point voltage. From Chapter 4, it is observed that the modulation signals are in terms of the sharing functions K_1, K_2, and K_3. By proper control of these sharing functions can control the node currents.

The neutral current is given by Eq. (6.2), the main objective of the scheme is to make the neutral current zero

$$I_2 = 0. \tag{6.4}$$

Substituting the expression for the switching function using Eqs. (4.29 – 4.37) in Eq. (6.4) and , assuming the sharing function K_3 to be unity and solving (6.4) for the

unknown K_1, gives the sharing function K_1 , which ensures zero neutral current. The expression for the sharing function K_1 is in terms of the two capacitor voltages and is given by

$$K_1 = \frac{V_{c1}}{V_{c2}} K_3 . \tag{6.5}$$

The determined sharing functions are substituted in Eqs. (4.29 – 4.37) to calculate the modulation functions. These modulation signals when modulated using the proposed carrier-based PWM generates switching signals, which when applied to the devices ensures zero neutral current as shown in Figure 6.2 (II).

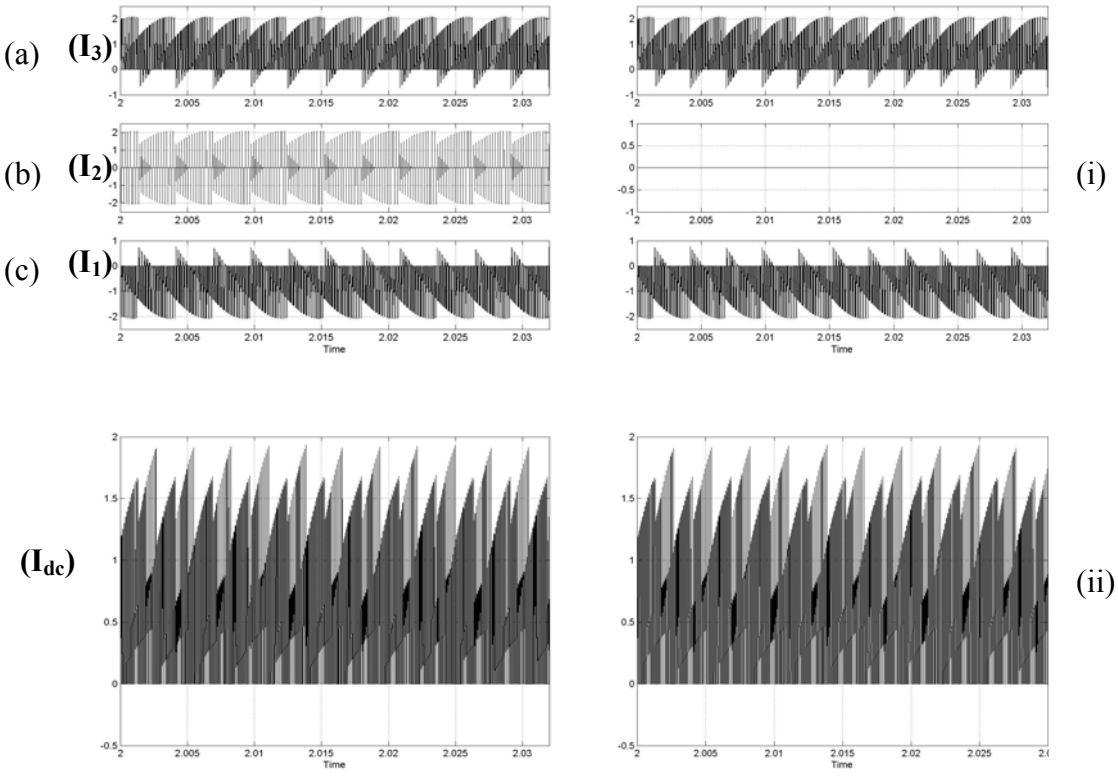


Figure 6.2: Control of neutral point current using the concept of sharing functions: (I) Without neutral current control (II) with neutral current control. (i) (a) Positive node current (I_3), (b) Neutral current (I_2), (c) Negative current, (ii) input dc current.

6.2.2 Four-level Inverter

In case of a four-level inverter, from Figure 6.3 it can be observed that there are four node currents I_4, I_3, I_2, and I_1.

The node currents of the inverter are given by

$$I_4 = H_{a4} i_a + H_{b4} i_b + H_{c4} i_c \tag{6.6}$$

$$I_3 = H_{a3} i_a + H_{b3} i_b + H_{c3} i_c \tag{6.7}$$

$$I_2 = H_{a2} i_a + H_{b2} i_b + H_{c2} i_c \tag{6.8}$$

$$I_1 = H_{a1} i_a + H_{b1} i_b + H_{c1} i_c . \tag{6.9}$$

In case of the four-level inverter, there is no neutral point available but in the steady-state operation, sum of the currents flowing through the positive should be equal to the sum of the currents flowing through the negative nodes. The capacitor voltages have to be maintained stiff to achieve this condition. From Chapter 4, it is known that there are four sharing functions K_1, K_2, K_3, and K_4, which influence the flow of currents through these nodes. For balanced condition, the following criteria have to be achieved:

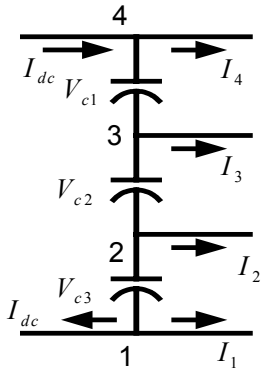


Figure 6.3 Schematic of a four level inverter.

$$I_1 = -I_4 \tag{6.10}$$

$$I_2 = -I_3. \tag{6.11}$$

Substituting the expression for the modulation signals in Eqs. (6.6 – 6.9) and solving Equations (6.10) and (6.11), gives

$$K_1 = \frac{V_{c1}K_3K_4}{K_3V_{c2} + (K_3 + K_4)V_{c3}} \tag{6.12}$$

$$K_2 = \frac{V_{c1}K_3K_4}{K_3(V_{c1} + V_{c2} + V_{c3}) - (V_{c1} + V_{c2})K_4}. \tag{6.13}$$

Assuming the sharing functions for K_3 and K_4, K_1 and K_2 can be evaluated. Substituting the sharing functions in [A.1], modulation signals can be obtained. When these signals are modulated using the proposed carrier-based PWM scheme achieves the desired conditions.

6.2.3 Five-Level Inverter

The neutral point is only available in odd number multilevel inverter. $I_{(N/2)-1}$ is considered as the neutral current. There are five node currents I_5, I_4, I_3, I_2, and I_1 as shown in Figure 6.4.

The node currents are given by

$$I_5 = H_{a5}i_a + H_{b5}i_b + H_{c5}i_c \tag{6.14}$$

$$I_4 = H_{a4}i_a + H_{b4}i_b + H_{c4}i_c \tag{6.15}$$

$$I_3 = H_{a3}i_a + H_{b3}i_b + H_{c3}i_c \tag{6.16}$$

$$I_2 = H_{a2}i_a + H_{b2}i_b + H_{c2}i_c \tag{6.17}$$

$$I_1 = H_{a1}i_a + H_{b1}i_b + H_{c1}i_c. \tag{6.18}$$

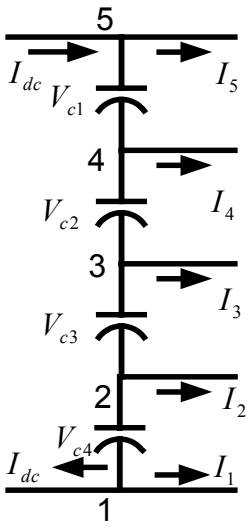


Figure 6.4: Schematic of five-level inverter.

To balance the flow of node currents and to make the neutral current to be zero, the following conditions have to be achieved:

$$I_5 = -I_1 \tag{6.19}$$

$$I_4 = -I_2. \tag{6.20}$$

There are five sharing functions K_1, K_2, K_3, K_4, and K_5. Substituting the expressions for the modulation signals which are in terms of the sharing functions in Eqs. (6.14 – 6.18) and solving Eq. (6.19) and (6.20) gives

$$K_2 = \frac{V_{c2}K_1K_4K_5}{K_1K_4(V_{c3}+V_{c4})-(V_{c2}+V_{c1})K_4K_5+K_1K_4V_{c3}} \tag{6.21}$$

$$K_3 = \frac{V_{c2}K_1K_4K_5}{-K_1K_4(V_{c2}+V_{c3}+V_{c4})+(V_{c2}+V_{c3})K_1K_5+K_5K_4V_{c1}}. \tag{6.22}$$

Assuming the sharing functions K_1 , K_4, and K_5, the sharing functions K_2 and K_3 can be evaluated using Eq. (6.21) and (6.22). By substituting these sharing functions in [A.2], the modulation signals can be obtained and the neutral can be controlled.

6.3 Control of Neutral Point Voltage Using the Generalized Discontinuous PWM

The general discontinuous modulation scheme presented in Chapter 4 is used in controlling the neutral point voltage. The generalized zero sequence voltage derived is used to control the neutral voltage. The space vector is divided into three different regions as shown in Figure 6.5 depending on the modulation index. Also based on the zero sequence voltage produced, each sector in the space vector is divided into positive and negative vectors. By continuously using the positive vectors, the upper capacitor charges to the dc bus voltage and the bottom capacitor discharges to zero and vice-versa. By proper selection of the vectors, the neutral voltage can be controlled.

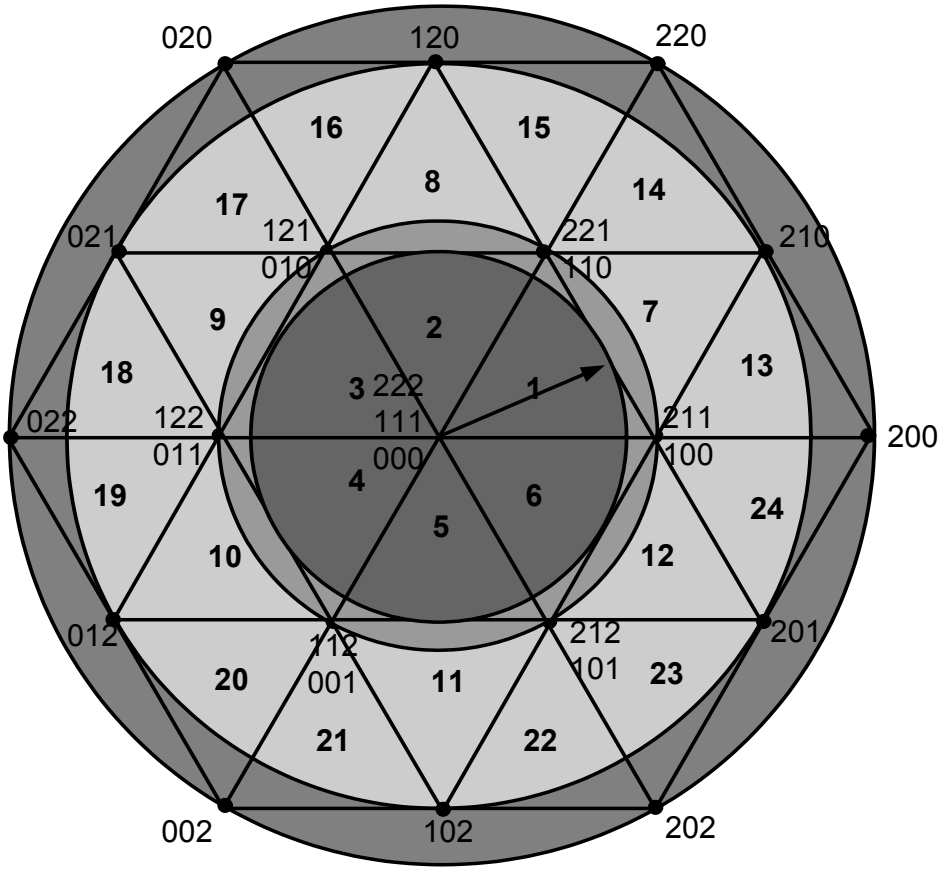
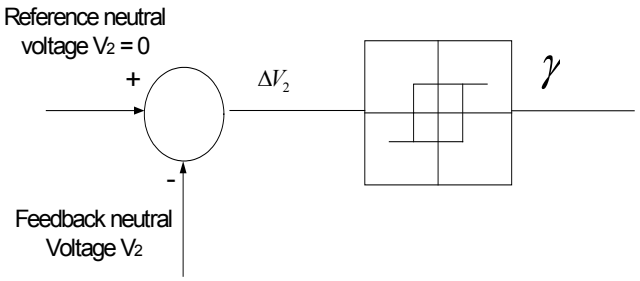


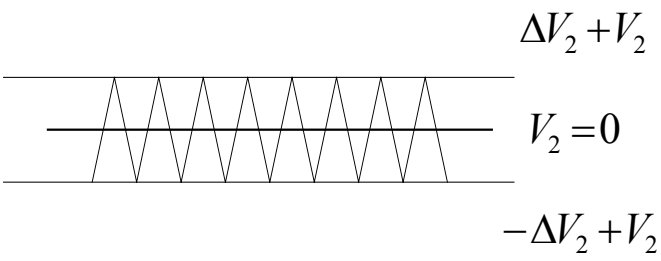
Figure 6.5: Different regions in the space vector diagram.

6.4 Hysteresis Control Scheme

The hysteresis current-control concept typically employed can be extended to multilevel systems by defining a number of hysteresis bands. The basic operation of the control involves defining two evenly spaced hysteresis bands on each side of the commanded neutral voltage shown in Figure 6.6 (II). The zero sequence voltage level is changed each time the measured voltage departs from the commanded value and crosses a hysteresis band. One important detail of this control is that the positive or negative zero sequence voltage is selected when the measured voltage crosses the lowermost or uppermost hysteresis band, respectively. The output of the hysteresis controller is considered as γ which takes a value 0 or 1 and decides on the selection of the vectors to be used. This ensures that the voltage will regulate about the commanded value. This straightforward voltage control results in good regulation of the voltages and acceptable voltage level switching [47]. Furthermore, the multilevel hysteresis control handles step changes in commanded voltage. There are many other methods of implementing hysteresis band based current controls for multilevel inverters. The dual hysteresis band approach has also been used in the four-level diode clamped rectifier where the inner band is used to achieve capacitor voltage balancing and the outer band is used for current regulation [50]. Two tolerance bands are defined around the reference current. The inner band schedules a switching event of the rectifier when the resulting capacitor current drives the voltage deviations to zero. If the same switching state can also drive the input current towards the reference, current regulation can also be achieved.



(I)



(II)

Figure 6.6: (I) Structure of hysteresis controller (II) the band of the neutral point voltage.

Figure 6.7 shows the schematic of the control scheme. A three-level inverter is connected to a balanced three-phase load. The actual neutral point voltage is compared with reference neutral voltage. The error signal is passed through the hysteresis controller and depending on the magnitude and polarity of the error signal, the hysteresis controller outputs γ, which selects the vectors to maintain the neutral voltage at the reference voltage.

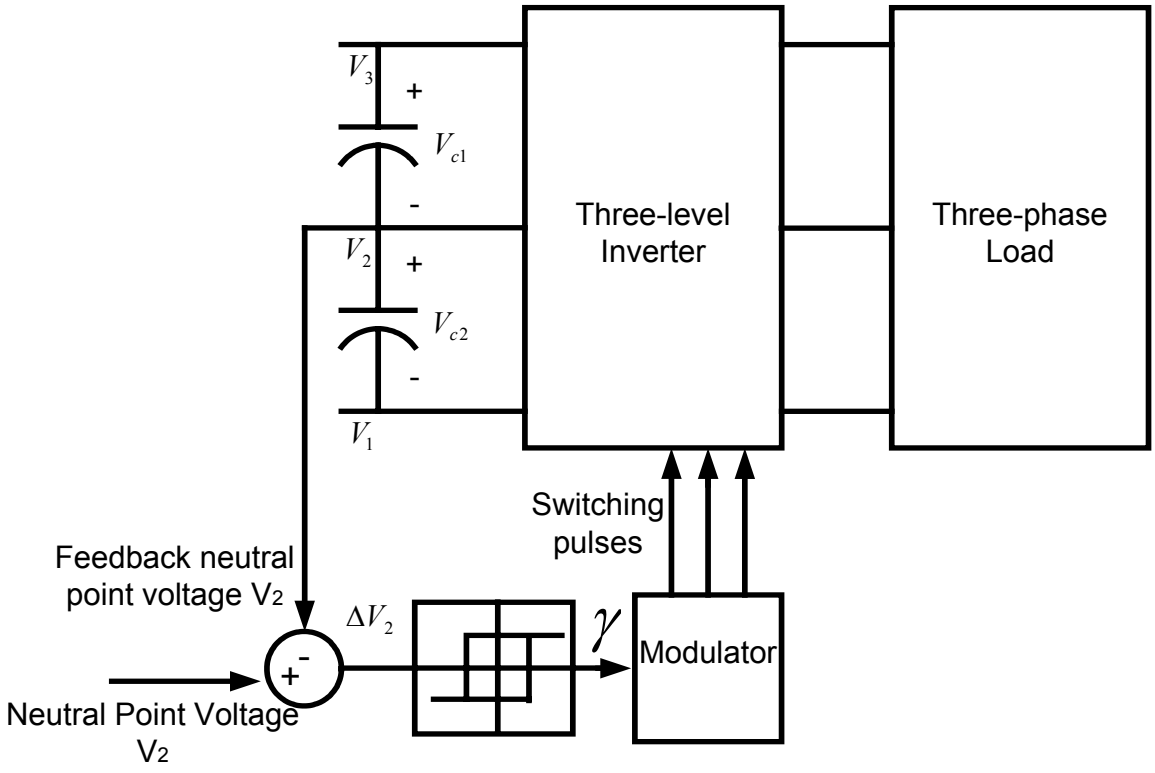


Figure 6.7: Schematic of the control scheme.

Region 1:

When the modulation index of the signals is less than 0.5, the reference voltage lies in the Region 1 i.e., to generate the reference voltage sectors 1-6 are used as shown in Figure 6.8. Region 1 has two zero sequence voltages as shown in Table 6.1 and hysteresis controller select between the positive and negative zero sequence voltage. This can be achieved using the control variable γ, which can take value either 1 or 0. Hence when γ = 1, positive vectors are selected and when γ = 0 negative vectors are selected. Obviously by continuously using only the positive zero sequence the upper capacitor gets fully charged as shown in Figure 6.9 (I) and by using only the negative zero sequence the lower capacitor gets fully charged as shown in Figure 6.9 (II). Hence whenever the

neutral point voltage V_2 reaches the upper band i.e., upper capacitor is charged more than the lower capacitor hence the hysteresis controller will output $\gamma = 0$ which selects the negative zero sequence and lets the lower capacitor charge and when V_2 reaches the lower the band $\gamma = 1$. Hence in Region 1 the neutral point voltage is controlled.

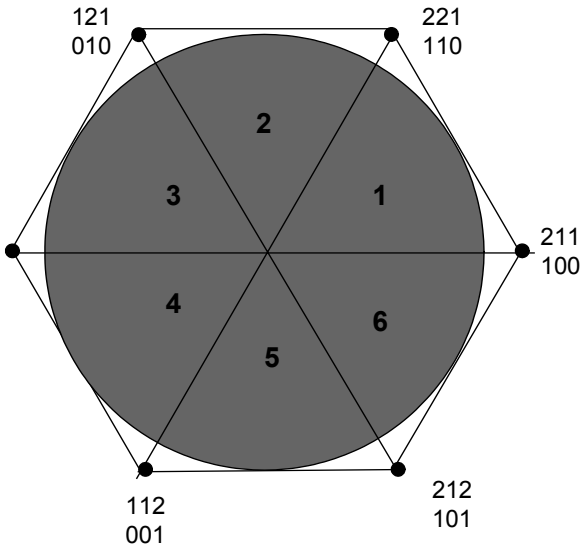


Figure 6.8: Region 1 of space vector diagram.

Table 6.1 Generalized zero sequence voltage for all sectors

Sectors	Generalized zero sequence expression	
1 - 6	$(2\alpha-1)V_{max}+\alpha V_{min}$	Positive zero sequence
	$-(\alpha-1)V_{max}-(2\alpha-1)V_{min}$	Negative zero sequence
7 - 12	$(1-\alpha)+(2\alpha-1)V_{max}+\alpha V_{min}$	Positive zero sequence
	$(1-\alpha)V_{max}+(1-2\alpha)V_{min}-\alpha$	Negative zero sequence
13 - 24	$(1-2\alpha)-(1-\alpha)V_{max}-(\alpha)V_{min}$	

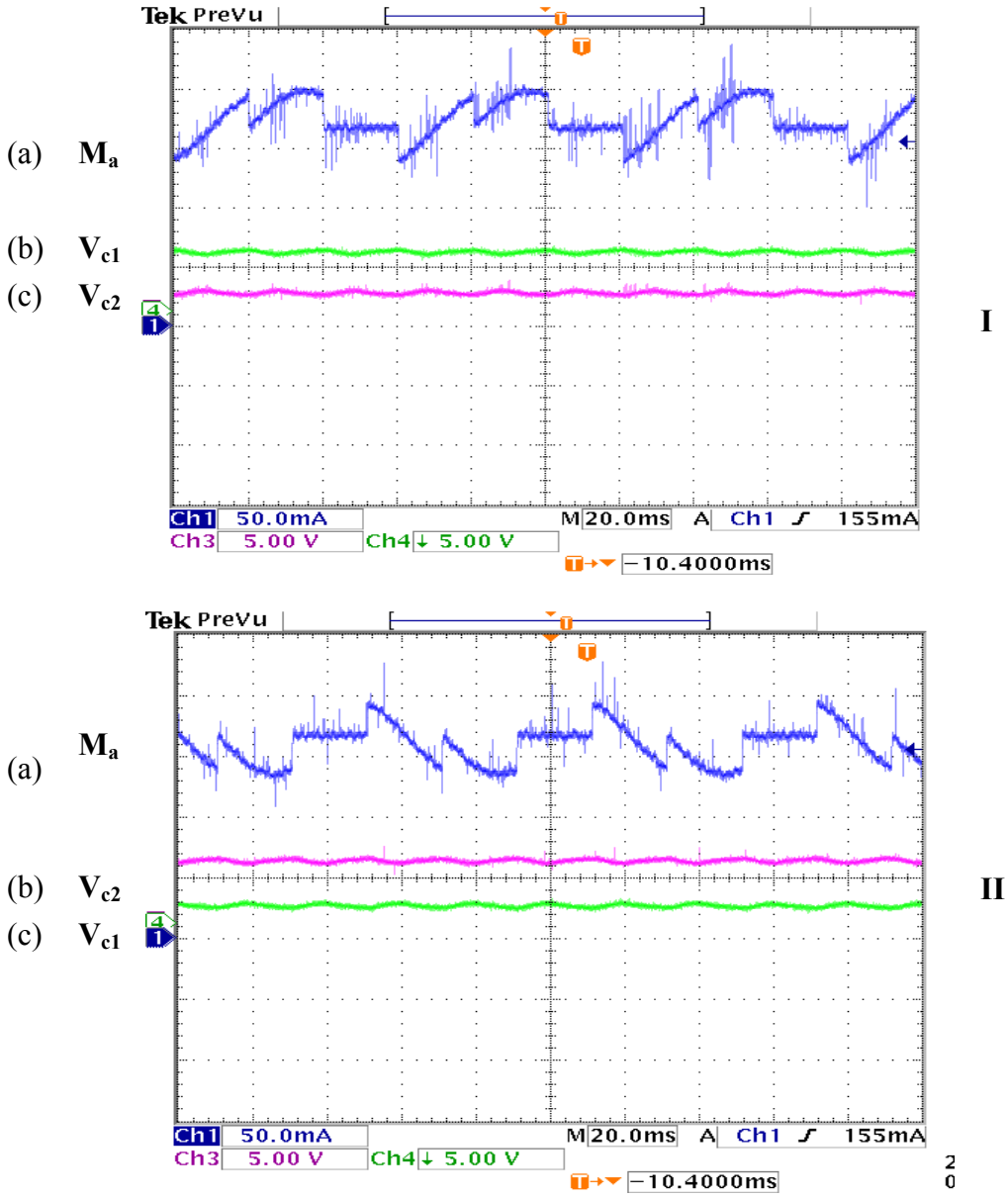


Figure 6.9: Control of the capacitor voltages in Region 1 of space vector diagram: For V_{dc} = 50 V (I) Using Positive zero sequence (a) Phase "a" modulation signal (b) Upper Capacitor Voltage V_{c1} (5 vol/div) (c) Lower capacitor voltage V_{c2} (5 vol/div) . (II) Using Negative zero sequence (a) Phase "a" modulation signal (b) Lower Capacitor Voltage V_{c2} (5 vol/div) (c) Upeer capacitor voltage V_{c1} (5 vol/div). Note: 10x probe was used and all quantities must be multiplied by 10 to get the actual values.

Region 2:

When the modulation index is greater than 0.5 and less than 0.63, the reference voltage lies in Region 2. The reference voltage travels through sectors from 1-12 as seen in Figure 6.10. In this region the zero sequence is taken as the average of sectors 1-6 and 7-12. Similar to Region 1, even in this region the control variable is γ which will in turn select the zero sequence voltage. Figure 6.11 (I) and (II) show that by continuously using the positive zero sequence the upper capacitor get fully charged and by using the negative zero sequence the bottom capacitor gets fully charged. Hence using this charging and discharging phenomenon the neutral voltage is controlled in Region 2.

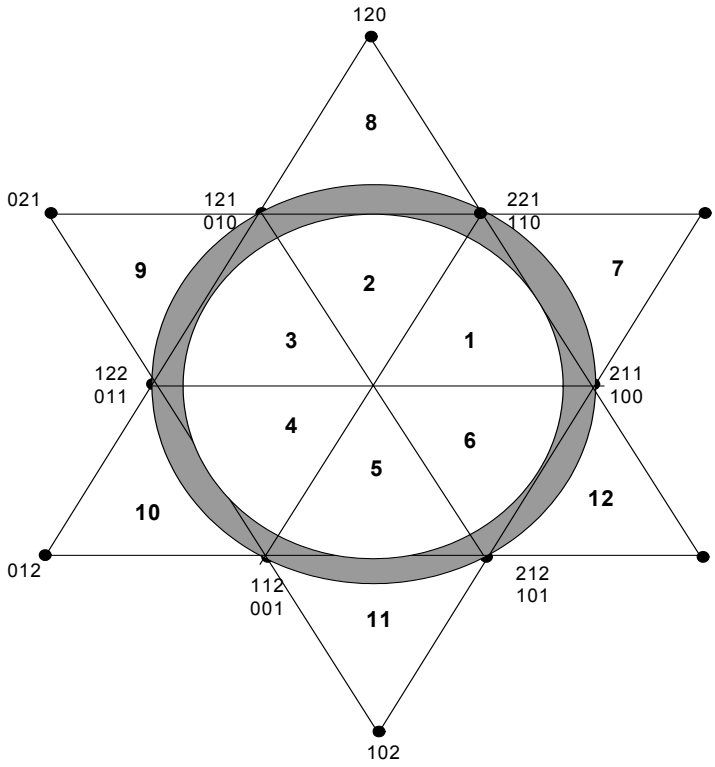


Figure 6.10: Region 2 of the space vector diagram.

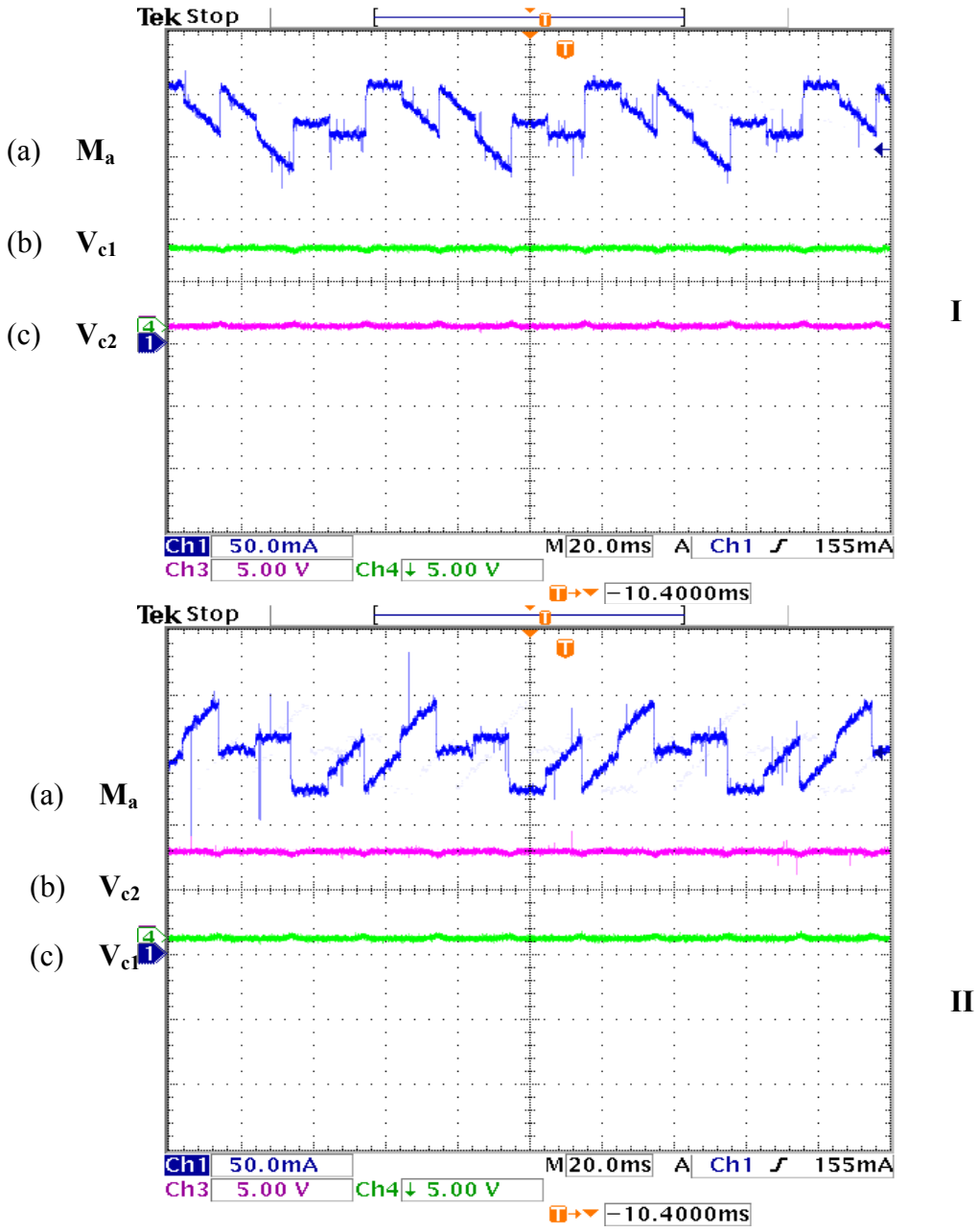


Figure 6.11: Control of the capacitor voltages in Region 2 of space vector diagram: For V_{dc} = 50 V. (I) Using Positive zero sequence (a) Phase "a" modulation signal (b) Upper Capacitor Voltage V_{c1} (5 vol/div) (c) Lower capacitor voltage V_{c2} (5 vol/div) . (II) Using Negative zero sequence (a) Phase "a" modulation signal (b) Lower Capacitor Voltage V_{c2} (5 vol/div) (c) Upper capacitor voltage V_{c1} (5 vol/div). 10x probe was used and all quantities must be multiplied by 10 to get the actual values.

Region 3:

When the modulation index is greater than 0.63 and less than 1, the reference voltage lies in Region 3. In this region sectors 7-24 are used to generate the reference voltage. For sectors 13-24 as seen from Table 6.1, it is clear that the zero sequence voltage is same as that of the two-level inverter. In this region the control variable γ is used to select between the positive and the negative vectors for sectors from 7-24.

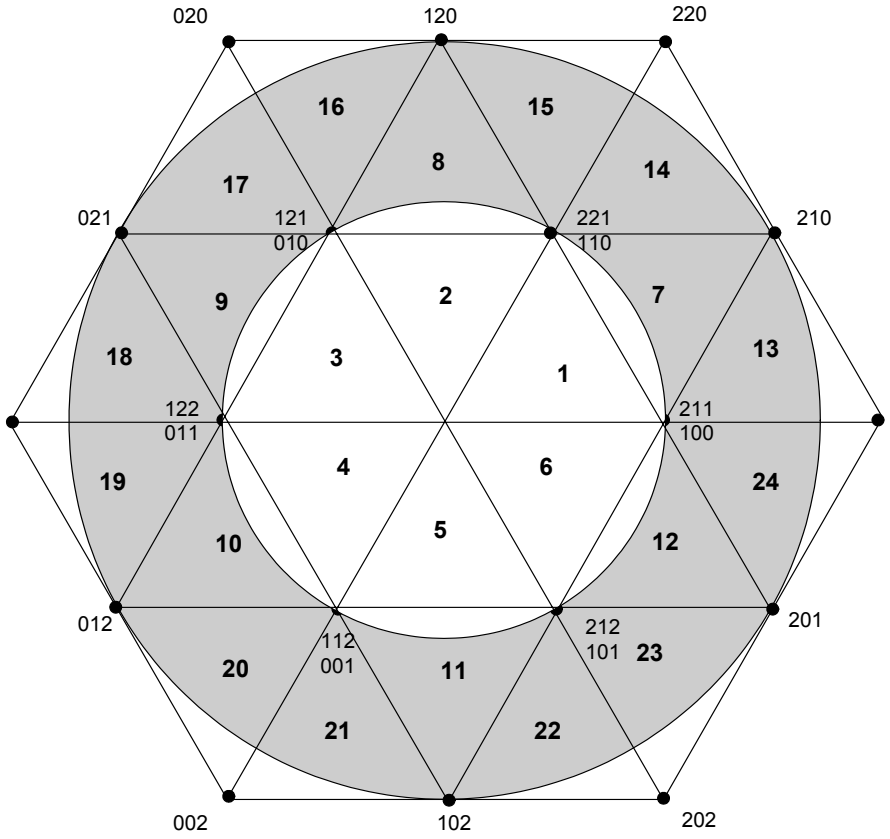


Figure 6.12: Region 3 of space vector diagram.

6.5 Experimental Results

The capacitors are been charged using the dc power supply. The neutral point voltage control scheme is being implemented in all the operating regions as explained in the previous sections. Figure 6.14 illustrates the experimental results of the control scheme in region I. Figure 6.14 (I) shows the capacitor voltage balancing, initially when there was no control scheme; one of the capacitor is charged fully to V_{dc} (in the present case V_{dc} was 100 V) and the other capacitor is charged to zero. But when the control scheme switched on after sometime, as it is clear from Figure 6.14 (I) the capacitor voltages are each brought to half the dc bus voltage with some ripple voltage. The ripple in the dc bus voltages is because of the control algorithm; when the neutral voltage reaches either of the band, the hysteresis controller makes the capacitors to charge or discharge and hence as the capacitors cannot respond to sudden changes in the voltages, it takes sometime to respond and hence keeps charging and after some time the directions change. The controller is so fast that the capacitor cannot respond to these fast change. Figure 6.14 (II) shows the zoomed picture of the capacitor voltages so as to explicitly show the ripple voltage. The ripple voltage in case of region 1 is around ±5 V. Figure 6.14 (III) (a) shows the line-line voltage and the (III) (b) phase "a" current. Figure 6.14 (IV) (a) shows the modulation signal and it can be seen that the modulation signal is clamped to the zero level for a certain period of time and hence the switching losses reduces because of the clamping. Figure 6.14 (IV) (b) shows the neutral current of the inverter. In the similar way Figures 6.15 and 6.16 illustrate the experimental results of the

neutral point voltage control in the region II and region III. It is clear from the results that the ripple voltage is more in region II when compared the other regions.

Control of neutral point voltage in region 1.

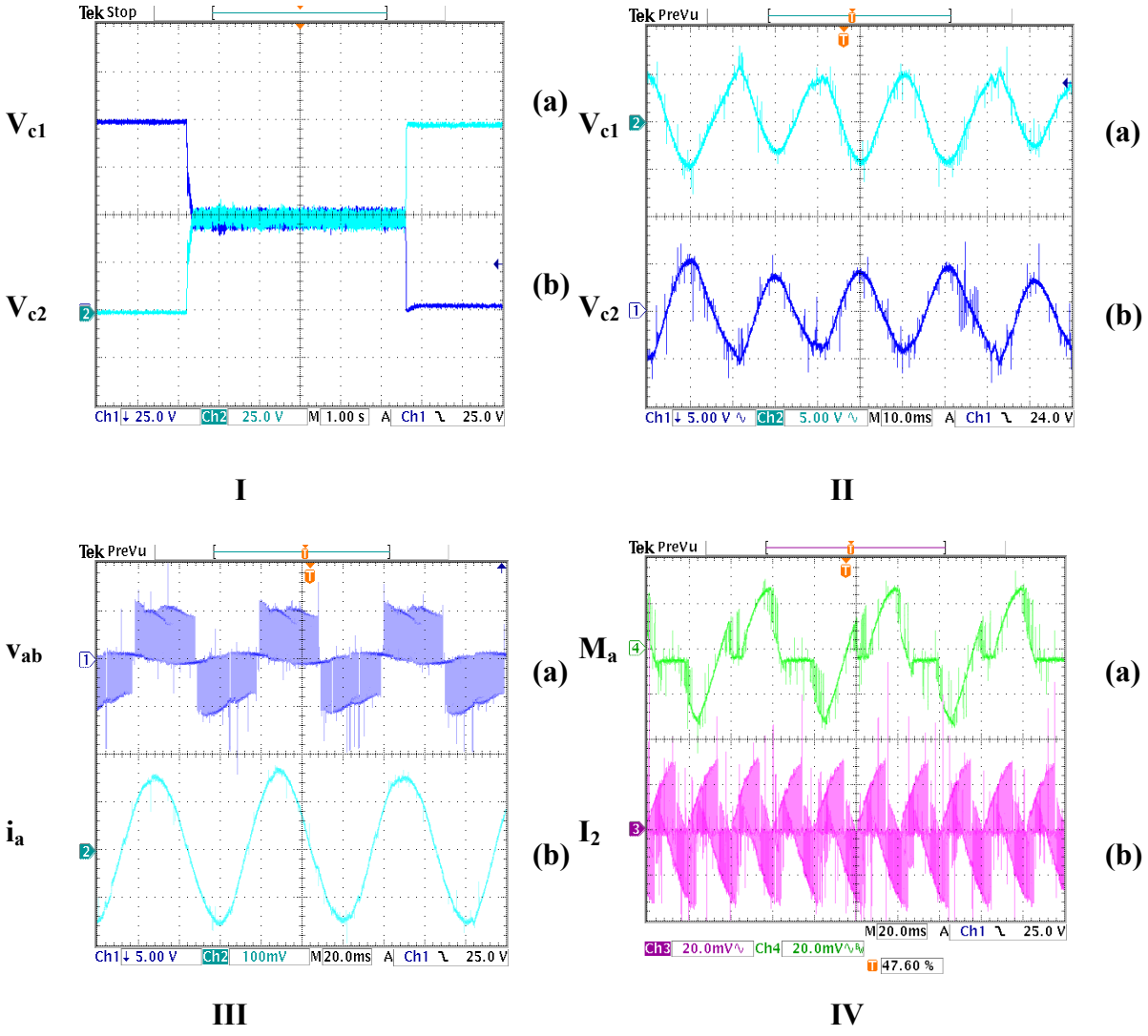


Figure 6.14: Experimental results of neutral point voltage control of three-level inverter for region 1.V_{dc} = 100 V. (I) (a) (b) Upper and lower capacitor voltage (25 V/div) (II) Zoomed in capacitor voltages (5 V/div) (III) (a) Line-line voltage (50 V/div) (b) Phase "a" current (1 A/div) (IV) Phase "a" modulation signal (b) Neutral current (0.5 A/div).

Control of neutral point voltage in region 2.

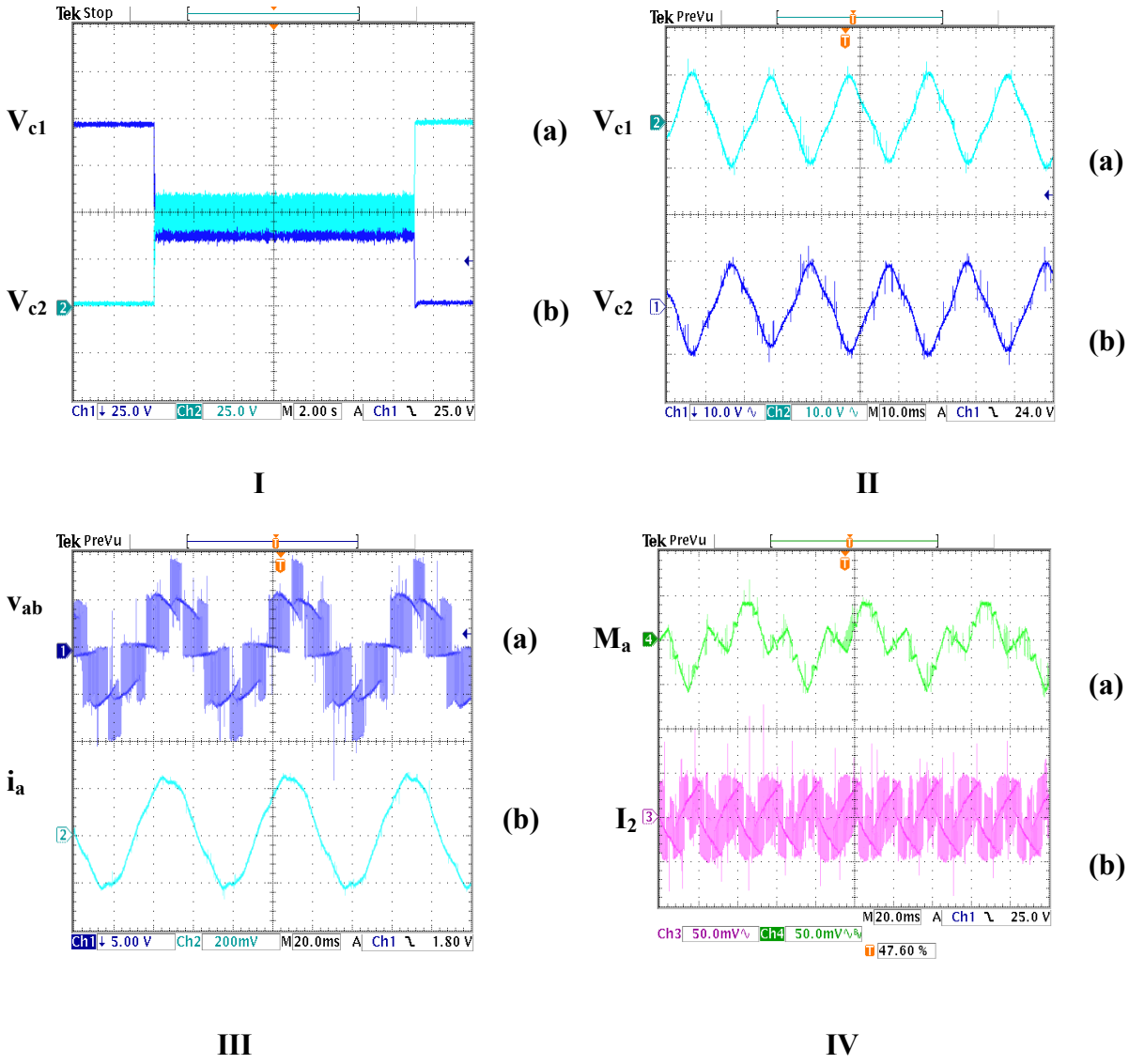


Figure 6.15: Experimental results of neutral point voltage control of three-level inverter for region 2. m_a = 0.6, V_{dc} = 100 V. (I) (a) (b) Upper and lower capacitor voltage (25 V/div) (II) Zoomed in capacitor voltages (10 V/div) (III) (a) Line-line voltage (50 V/div) (b) Phase "a" current (1 A/div) (IV) Phase "a" modulation signal (b) Neutral current (1 A/div).

Control of neutral point voltage in region 3.

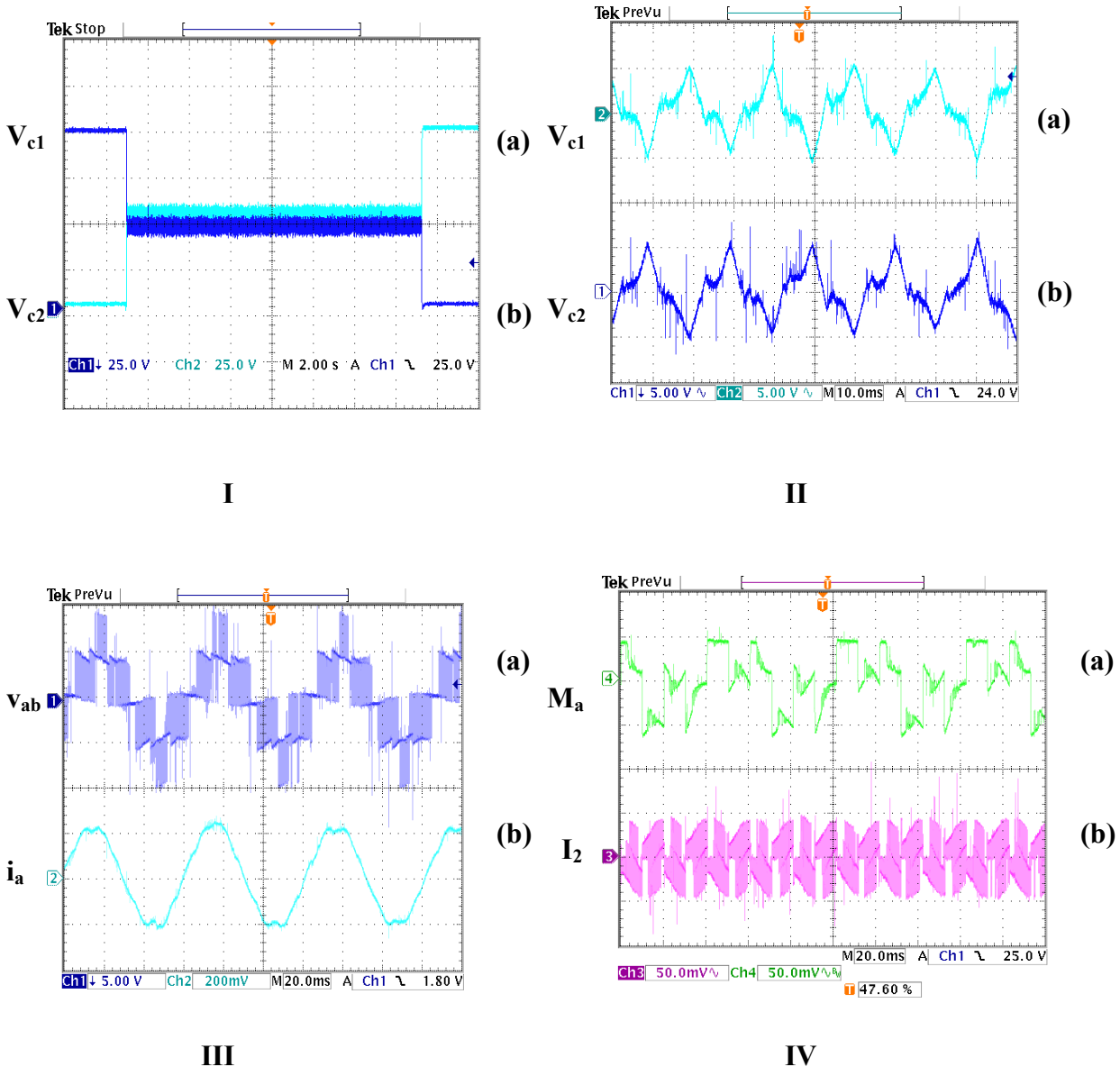


Figure 6.16: Experimental results of neutral point voltage control of three-level inverter in region 3. m_a = 0.9, V_{dc} = 100 V. (I) (a) (b) Upper and lower capacitor voltage (25 V/div), (II) Zoomed in capacitor voltages (5 V/div), (III) (a) Line-line voltage (50 V/div) (b) Phase "a" current (1 A/div), (IV) Phase "a" modulation signal (b) Neutral current (1 A/div).

6.6 Neutral Point Voltage Control under Unbalanced Load

One of the main causes for the neutral point voltage is due to the unbalanced load conditions. Due to unbalance loads, load currents drawn in the phases have different peaks. In the present case, the load is assumed to be comprised of R, L, and E. Figures 6.17 – 6.19 illustrate the simulation results for unbalanced load for three different regions. The simulation results for region 3 are shown in Figure 6.17. In the simulation, initially the band of the hysteresis is assumed to be large and after a period of time the band is reduced so as to verify the effectiveness of the controller. Figure 6.17 (a) shows the modulation signal required to obtain the neutral point voltage. Figure 6.17 (b) shows the capacitor voltages, which have initially, high ripple voltage and when the hysteresis band is reduced the ripple in the capacitor voltage is reduced. Figure 6.17 (c) gives the line –line voltage and it can be seen that initially the waveform had some ripple due to high band and when the band is reduced at t = 0.3 sec the waveform was improved. Figure 6.17 (d) illustrates the three-phase currents and from the figure it can be seen that the peaks of the currents are different for all phases. Figure 6.17 (e) represent the neutral point voltage and it can be seen that initially the ripple was around 20 V and after the hysteresis band is reduced the ripple reduced to around 3 V. This shows the effectiveness of the hysteresis controller. Similarly Figures 6.18 and 6.19 illustrate the simulation results for region 2 and region 1, respectively.

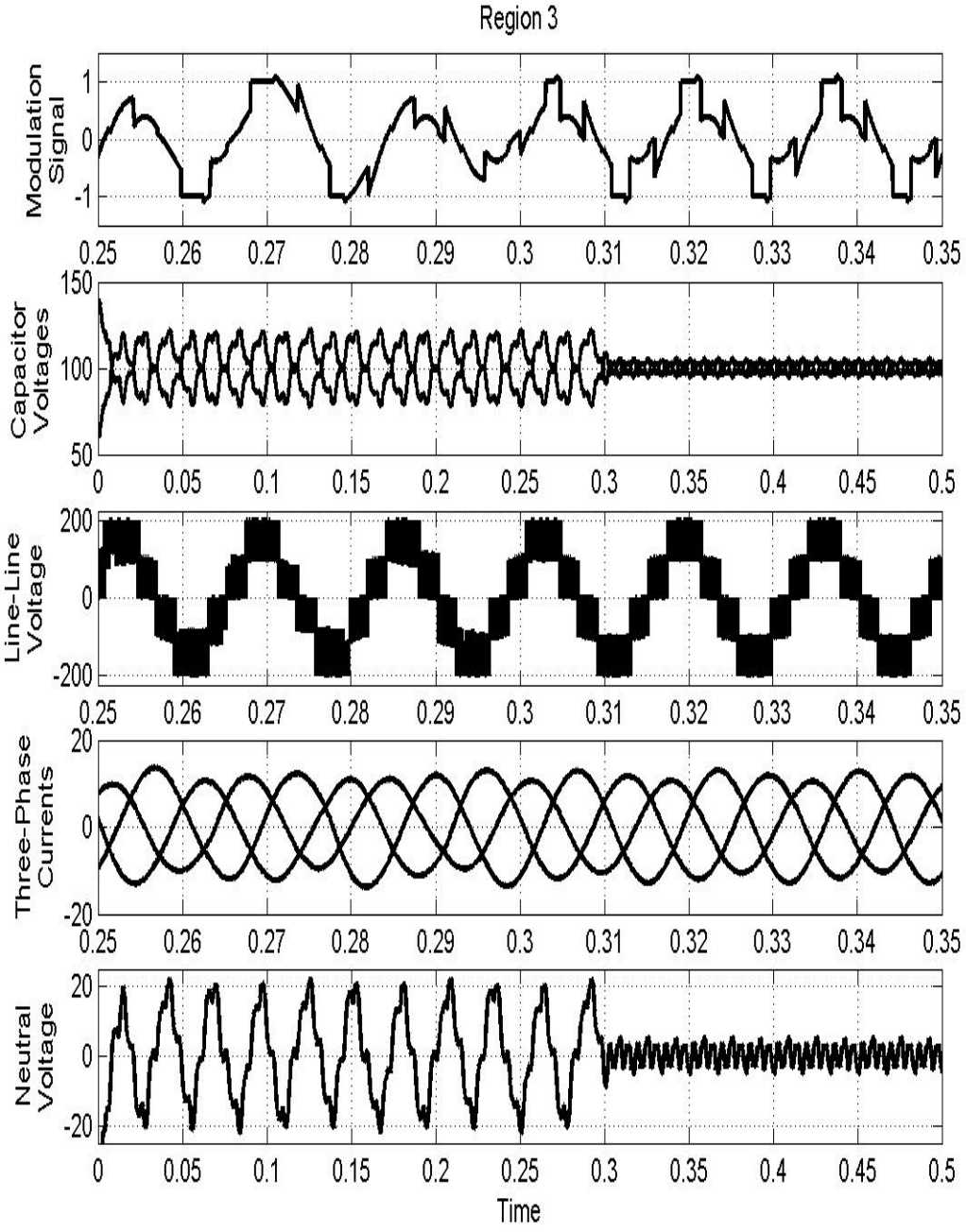


Figure 6.17: Neutral point voltage control under unbalanced load condition for Region 3 (a) Modulation signal (b) Capacitor voltages (V_{c1}, V_{c2}) (c) Line-line voltage (V_{ab}) (d) Three-phase currents (e) Neutral point voltage.

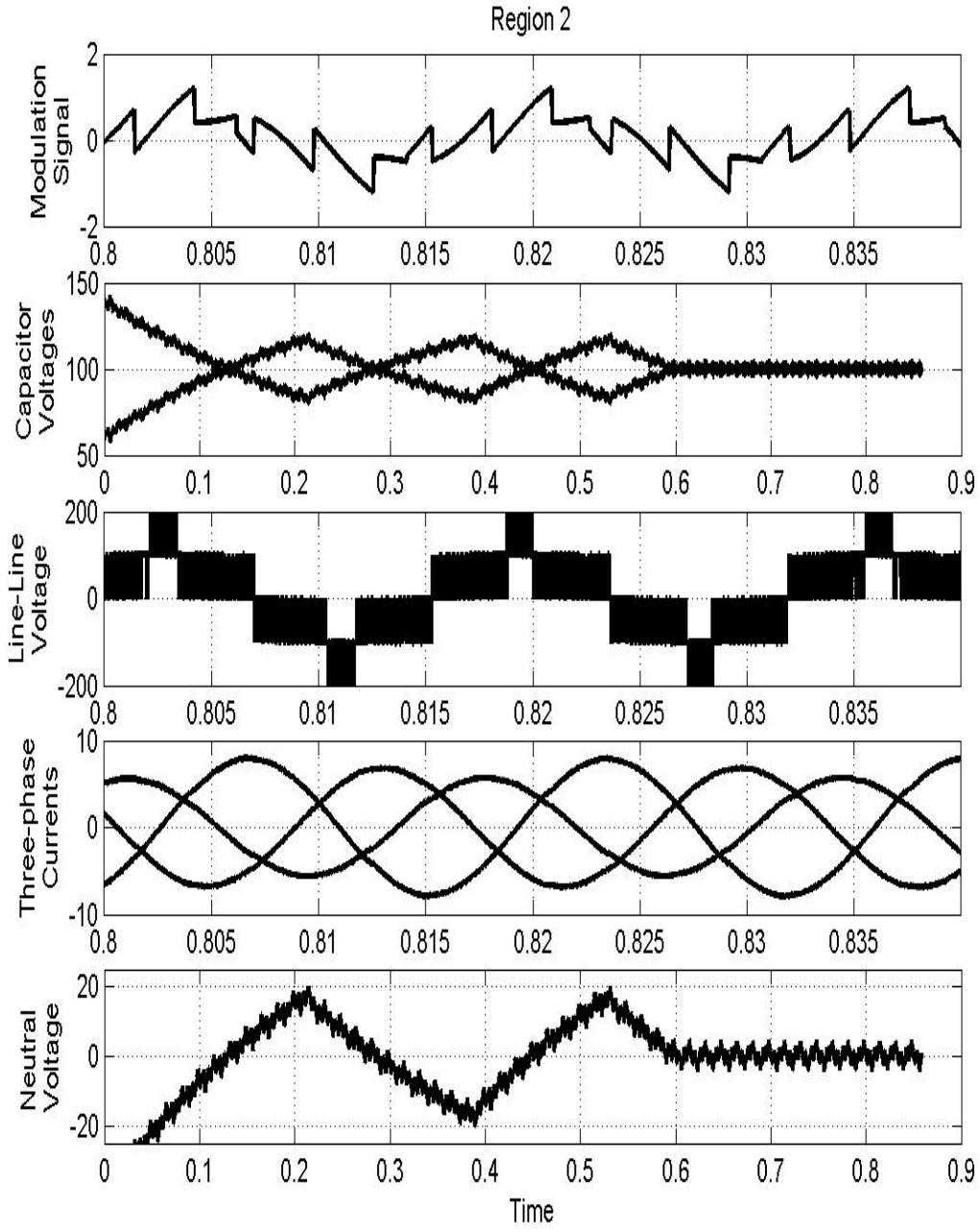


Figure 6.18: Neutral point voltage control under unbalanced load condition for Region 2 (a) Modulation signal (b) Capacitor voltages (V_{c1}, V_{c2}) (c) Line-line voltage (V_{ab}) (d) Three-phase currents (e) Neutral point voltage.

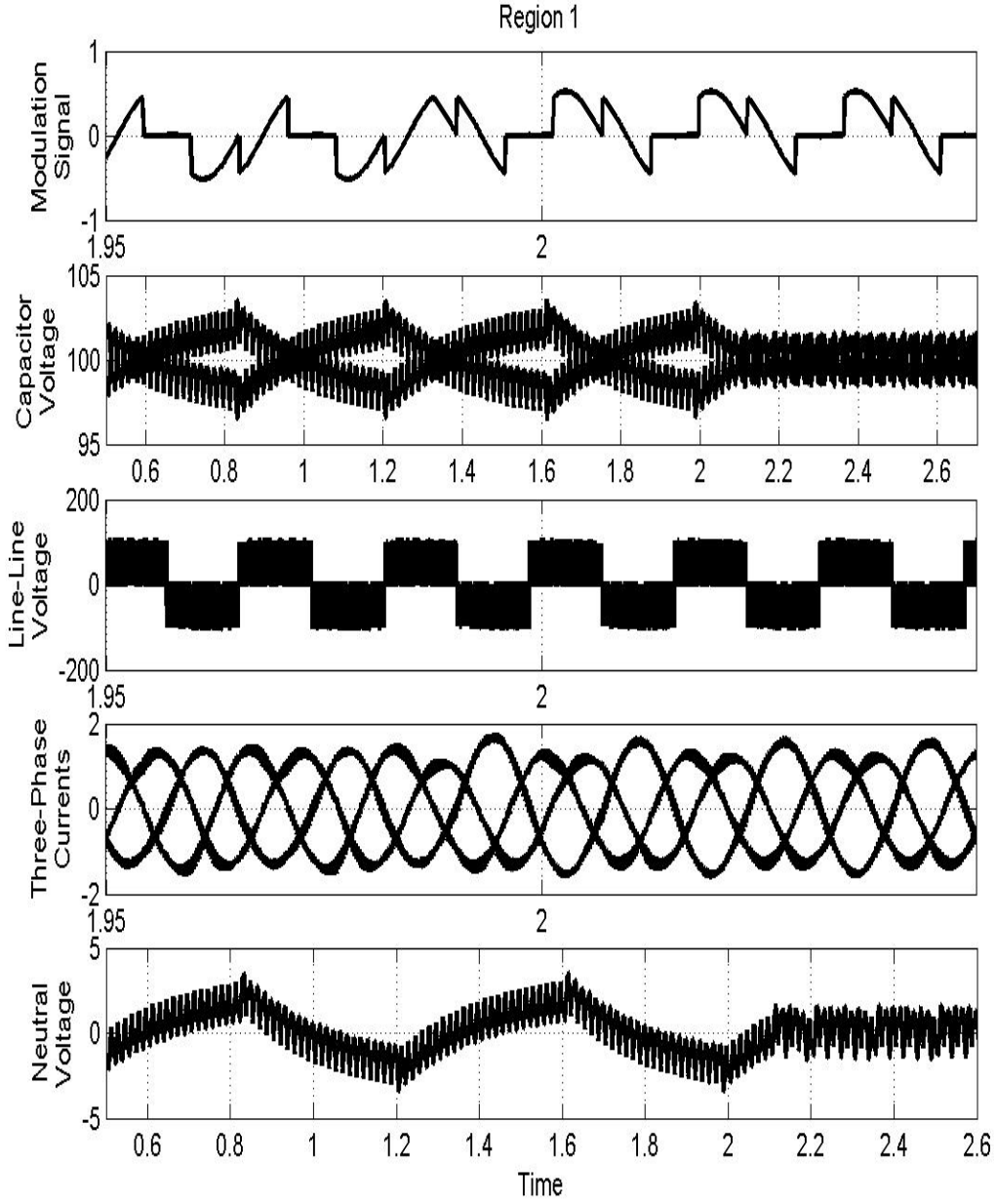


Figure 6.19: Neutral point voltage control under unbalanced load condition for Region 1 (a) Modulation signal (b) Capacitor voltages (V_{c1}, V_{c2}) (c) Line-line voltage (V_{ab}) (d) Three-phase currents (e) Neutral point voltage.